# Lesson Plan for the Session Summer-2023
## (4th SEMESTER CSE)

| DISCIPLINE: Computer Science & Engineering | SEMESTER: 4TH | NAME OF THE TEACHING FACULTY: MR PRAMOD KUMAR SWAIN |
|---|---|---|
| SUBJECT: Operating System | NO. OF DAYS/PER WEEK CLASS ALLOTTED: 4 | SEMESTER DURATION: 14/02/2023 TO DATE: 23/05/2023 NO.OF WEEKS : 15 |
| WEEK | CLASSDAY | THEORY/PRACTICALTOPICS |
| 1ST | 1ST | Objectives and Explain functions of operating system. |
| | 2ND | Evolution of Operating system |
| | 3RD | Structure of operating system |
| | 4TH | PROCESSMANAGEMENT<br>Process concept |
| 2ND | 1ST | process control, interacting processes |
| | 2ND | inter process messages. |
| | 3RD | Implementation issues of Processes. |
| | 4TH | Process scheduling |
| 3RD | 1ST | Job scheduling |
| | 2ND | Process synchronization |
| | 3RD | semaphore |
| | 4TH | Principle of concurrency |
| 4TH | 1ST | types of scheduling |
| | 2ND | MEMORY MANAGEMENT<br>Memory allocation Techniques |
| | 3RD | Contiguous memory allocation |
| | 4TH | non contiguous memory allocation |
| 5TH | 1ST | Swapping |
| | 2ND | Paging |
| | 3RD | Segmentation, |
| | 4TH | virtual memory using paging, |
| 6TH | 1ST | Demand paging |
| | 2ND | page fault handling |
| | 3RD | DEVICEMANAGEMENT |
| | 4TH | Techniques for Device Management |
| 7TH | 1ST | Dedicated |
| | 2ND | shared ,virtual |
| | 3RD | Device allocation considerations I/O traffic control |
| | 4TH | I/O Schedule |
| 8TH | 1ST | I/O Device handlers. |
| | 2ND | SPOOLING |
| | 3RD | DEADLOCKS |
| | 4TH | Concept of deadlock |

| | | |
|---|---|---|
| 9TH | 1ST | Types of deadlock |
| | 2ND | Dead Lock Detection |
| | 3RD | Resources allocation Graph |
| | 4TH | Methods of Deadlock handling |
| 10TH | 1ST | Recovery &Prevention |
| | 2ND | Explain Bankers Algorithm |
| | 3RD | Safety Algorithm |
| | 4TH | FILEMANAGEMENT |
| 11TH | 1ST | File organization |
| | 2ND | Directory & file structure |
| | 3RD | sharing of files |
| | 4TH | File access methods |
| 12TH | 1ST | file systems |
| | 2ND | reliability |
| | 3RD | Allocation of disk space |
| | 4TH | File protection |
| 13TH | 1ST | secondary storage management |
| | 2ND | SYSTEMPROGRAMMING |
| | 3RD | Concept of system programming |
| | 4TH | and show difference from Application Complier |
| 14TH | 1ST | Compiler |
| | 2ND | Concept of compiler |
| ` | 3RD | functions of compiler |
| | 4TH | functions of interpreter |
| 15TH | 1ST | Compare compiler and interpreter |
| | 2ND | Seven phases of compiler |
| | 3RD | Seven phases of compiler |
| | 4TH | brief description of each phase |

13/02/23
Signature of Faculty

13/2/2023
HoD(I/c)
CSE Dept.

| DISCIPLINE: Computer Science & Engineering | SEMESTER: 4TH | NAME OF THE TEACHING FACULTY: MRS YOGESWARI MAGAR |
|---|---|---|
| SUBJECT: Data Communication and Computer Network | NO. OF DAYS/PER WEEK CLASS ALLOTTED: 4 | SEMESTER DURATION: 14/02/2023 TO DATE: 23/05/2023 NO.OF WEEKS : 15 |
| WEEK | CLASSDAY | THEORY/PRACTICALTOPICS |
| 1ST | 1ST | Network |
| | 2ND | Protocol |
| | 3RD | Data Communication |
| | 4TH | Architecture |
| 2ND | 1ST | Standards |
| | 2ND | OSI |
| | 3RD | TCP/IP |
| | 4TH | Data Transmission &Media |
| 3RD | 1ST | Data transmission Concepts and Terminology |
| | 2ND | Analog and Digital Data transmission |
| | 3RD | Transmission impairments |
| | 4TH | Channel capacity |
| 4TH | 1ST | Transmission media |
| | 2ND | Guided Transmission |
| | 3RD | Wireless Transmission |
| | 4TH | Data Encoding |
| 5TH | 1ST | Concept of Data Encoding |
| | 2ND | Digital data digital signals |
| | 3RD | Digital data analog signals |
| | 4TH | Analog data digital signals |
| 6TH | 1ST | Analog data analog signals |
| | 2ND | Data Communication & Data link control |
| | 3RD | Asynchronous and Synchronous Transmission |
| | 4TH | Error Detection |
| 7TH | 1ST | Line configuration |
| | 2ND | Flow Control |
| | 3RD | Error Control |
| | 4TH | Multiplexing |
| 8TH | 1ST | FDM synchronous TDM |
| | 2ND | Statistical TDM |
| | 3RD | Switching &Routing |
| | 4TH | Circuit Switching networks |
| 9TH | 1ST | Packet Switching principles |
| | 2ND | X.25 |

| | | |
|---|---|---|
| | 3RD | Routing in Packet switching |
| | 4TH | Congestion |
| 10TH | 1ST | Effects of congestion |
| | 2ND | Congestion control |
| | 3RD | Congestion control |
| | 4TH | Traffic Management |
| 11TH | 1ST | Congestion Control in Packet Switching Network |
| | 2ND | LAN Technology |
| | 3RD | Topology |
| | 4TH | Transmission Media |
| 12TH | 1ST | LAN protocol architecture |
| | 2ND | Medium Access control |
| | 3RD | Medium Access control |
| | 4TH | Bridges, Hub, Switch |
| 13TH | 1ST | Ethernet (CSMA/CD), |
| | 2ND | Ethernet (CSMA/CD), |
| | 3RD | CSMA/CA |
| | 4TH | Fiber Channel |
| 14TH | 1ST | Wireless LAN Technology |
| | 2ND | TCP/IP |
| ` | 3RD | TCP/IP Protocol Suite |
| | 4TH | Basic Protocol functions |
| 15TH | 1ST | Principles of Inter networking |
| | 2ND | Principles of Inter networking |
| | 3RD | Internet Protocol operations |
| | 4TH | Internet Protocol |

13/12/23.

Signature of Faculty

13/12/2023

HoD(I/c)
CSE Dept.

| DISCIPLINE: Computer Science & Engineering | SEMESTER: 4TH | NAME OF THE TEACHING FACULTY: MRS LIPIKA SANDHA |
|---|---|---|
| SUBJECT: MICROPROCESSOR & MICROCONTROLLER | NO. OF DAYS/PER WEEK CLASS ALLOTTED: 4 | SEMESTER DURATION: 14/02/2023 TO DATE: 23/05/2023 NO.OF WEEKS : 15 |
| WEEK | CLASSDAY | THEORY/PRACTICALTOPICS |
| 1ST | 1ST | Microprocessor |
| | 2ND | Introduction to Microprocessor and Microcomputer & distinguish between them. |
| | 3RD | Concept of Address bus, data bus, control bus & System Bus |
| | 4TH | General Bus structure Block diagram. |
| 2ND | 1ST | Basic Architecture of 8085 (8 bit)Microprocessor |
| | 2ND | Basic Architecture of 8085 (8 bit)Microprocessor |
| | 3RD | Signal Description (Pin diagram) of 8085Microprocessor |
| | 4TH | Signal Description (Pin diagram) of 8085Microprocessor |
| 3RD | 1ST | Register Organizations, Distinguish between SPR & GPR, Timing & Control Module,) |
| | 2ND | Interrupts:-8085 Interrupts, Masking of Interrupt(SIM,RIM |
| | 3RD | Interrupts:-8085 Interrupts, Masking of Interrupt(SIM,RIM |
| | 4TH | Addressing data & Differentiate between one-byte, two-byte &three-byte instructions with examples |
| 4TH | 1ST | Addressing data & Differentiate between one-byte, two-byte &three-byte instructions with examples |
| | 2ND | Addressing data & Differentiate between one-byte, two-byte &three-byte instructions with examples |
| | 3RD | Addressing modes in instructions with suitable examples |
| | 4TH | Addressing modes in instructions with suitable examples |
| 5TH | 1ST | Instruction Set of 8085(Data Transfer, Arithmetic, Logical, Branching, Stack& I/O , Machine Control) |
| | 2ND | Instruction Set of 8085(Data Transfer, Arithmetic, Logical, Branching, Stack& I/O , Machine Control) |
| | 3RD | Simple Assembly Language Programming of8085 Simple Addition &Subtraction |
| | 4TH | Logic Operations (AND, OR, Complement 1's & 2's) & Masking of |
| 6TH | 1ST | Counters & Time delay (Single Register, Register Pair, More than Two Register) |
| | 2ND | Looping, Counting & Indexing (Call/JMP etc). |
| | 3RD | Stack &Subroutines programs, Code conversion, BCD Arithmetic & 16 Bit data Operation, Block Transfer. |
| 7TH | 1ST | Memory & I/O Addressing |
| | 2ND | TIMINGDIAGRAMS |

| | | |
|---|---|---|
| | 3RD | Define op code, operand, T-State, Fetch cycle, Machine Cycle, Instruction cycle& discuss the concept of timing diagram. |
| | 4TH | Draw timing diagram for memory read, memory write, I/O read, I/O write machine cycle. |
| 8TH | 1ST | Draw a neat sketch for the timing diagram for 8085 instruction(MOV,MVI,LDA instruction). |
| | 2ND | Draw a neat sketch for the timing diagram for 8085 instruction(MOV,MVI,LDA instruction). |
| | 3RD | Microprocessor Based System Development Aids<br>Concept of interfacing |
| | 4TH | Define Mapping &Data transfer mechanisms -<br>Memory mapping & I/O Mapping<br>Concept of Memory Interfacing:- Interfacing EPROM & RAM Memories |
| 9TH | 1ST | Concept of Address decoding for I/O devices<br>Programmable Peripheral Interface:8255 |
| | 2ND | ADC & DAC with Interfacing |
| | 3RD | Draw a neat sketch for the timing diagram for 8085 instruction(MOV,MVI,LDA instruction). |
| | 4TH | Interfacing Seven Segment Displays |
| 10TH | 1ST | Generate square waves on all lines of8255<br>Design Interface a traffic light control system using8255. |
| | 2ND | Microprocessor (Architecture and Programming-16 bit-8086) |
| | 3RD | Register Organization of8086<br>Internal architecture of8086 |
| | 4TH | Signal Description of 8086<br>General Bus Operation& Physical Memory Organization |
| 11TH | 1ST | Minimum Mode& Timings, Maximum Mode& Timings |
| | 2ND | Interrupts and Interrupt Service Routines, Interrupt Cycle, |
| | 3RD | Non-Maskable Interrupt, Maskable Interrupt |
| | 4TH | 8086 Instruction Set & Programming: Addressing Modes, Instruction Set, Assembler Directives and Operators |
| 12TH | 1ST | 8086 Instruction Set & Programming: Addressing Modes, Instruction Set, Assembler Directives and Operators |
| | 2ND | Simple Assembly language programming using 8086instructions. |
| | 3RD | Simple Assembly language programming using 8086instructions. |
| | 4TH | Distinguish between Microprocessor &Microcontroller<br>8 bit & 16 bit microcontroller |
| 13TH | 1ST | CISC & RISC processor<br>Architectureof8051Microcontroller |
| | 2ND | Signal Descriptionof8051Microcontrollers<br>Memory Organization-RAM structure, SFR |
| | 4TH | Simple 8051 Assembly Language Programming<br>Arithmetic& Logic Instructions , JUMP, LOOP, CALL |

| | | |
|---|---|---|
| | | Instructions, I/O Port Programming |
| | 2ND | Simple 8051 Assembly Language Programming<br>Arithmetic& Logic Instructions , JUMP, LOOP, CALL Instructions, I/O Port Programming |
| | 3RD | Interrupts |
| | 4TH | Timer &Counters |
| 15TH | 1ST | Timer &Counters |
| | 2ND | Serial Communication |
| | 3RD | Microcontroller Interrupts and Interfacing to8255 |
| | 4TH | Microcontroller Interrupts and Interfacing to8255 |

11/02/2023
Signature of Faculty

13/2/2023
HoD(I/c)
CSE Dept.

| DISCIPLINE: Computer Science & Engineering | SEMESTER: 4TH | NAME OF THE TEACHING FACULTY: MRS MOUSUMI SUBUDHI |
|---|---|---|
| SUBJECT: DATABASE MANAGEMENT SYSTEM | NO. OF DAYS/PER WEEK CLASS ALLOTTED: 4 | SEMESTER DURATION: 14/02/2023 TO DATE: 23/05/2023 NO.OF WEEKS : 15 |
| WEEK | CLASSDAY | THEORY/PRACTICALTOPICS |
| 1ST | 1ST | BASIC CONCPETS OFDBMS<br>Purpose of database Systems |
| | 2ND | Explain Data abstraction |
| | 3RD | Data base users |
| | 4TH | Data definition language |
| 2ND | 1ST | Data Dictionary |
| | 2ND | Data independence |
| | 3RD | Entity relationship models |
| | 4TH | Entity sets and Relationship sets |
| 3RD | 1ST | Explain Attributes<br>Mapping constraints |
| | 2ND | E-R Diagram |
| | 3RD | E-R Diagram |
| | 4TH | Relational model |
| 4TH | 1ST | Hierarchical model |
| | 2ND | Network model |
| | 3RD | RELATIONALDATABASE<br>Introduction |
| | 4TH | Relation alalgebra |
| 5TH | 1ST | Different operators select, project, join , simple Examples |
| | 2ND | Different operators select, project, join , simple Examples |
| | 3RD | Different operators select, project, join , simple Examples |
| | 4TH | NORMALIZATION IN RELATIONALSYSTEM<br>Introduction |
| 6TH | 1ST | Functional Dependencies |
| | 2ND | Functional Dependencies |
| | 3RD | Lossless join |
| | 4TH | Importance of normalization |
| 7TH | 1ST | Compare First second and third normal forms |
| | 2ND | Compare First second and third normal forms |
| | 3RD | Compare First second and third normal forms |
| | 4TH | Explain BCNF |
| 8TH | 1ST | Explain BCNF |
| | 2ND | STRUCTURED QUERYLANGUAGE<br>Introduction |
| | 3RD | Elementary idea of Query language |

| | | |
|---|---|---|
| | 4TH | Queries in SQL |
| 9TH | 1ST | Queries in SQL |
| | 2ND | Simple queries to create, update, insert in SQL |
| | 3RD | Simple queries to create, update, insert in SQL |
| | 4TH | Simple queries to create, update, insert in SQL |
| | 2ND | Simple queries to create, update, insert in SQL |
| | 3RD | TRANSACTION PROCESSINGCONCEPTS Introduction |
| | 4TH | Idea about transaction processing |
| 11TH | 1ST | Transaction & system concept |
| | 2ND | Transaction & system concept |
| | 3RD | Desirable properties of transaction |
| | 4TH | Desirable properties of transaction |
| 12TH | 1ST | Schedules and recoverability |
| | 2ND | Schedules and recoverability |
| | 3RD | CONCURRENCY CONTROLCONCEPTS |
| | 4TH | Basic concepts |
| 13TH | 1ST | Locks, Live Lock, Dead Lock, |
| | 2ND | Locks, Live Lock, Dead Lock, |
| | 3RD | Locks, Live Lock, Dead Lock, |
| | 4TH | Locks, Live Lock, Dead Lock, |
| 14TH | 1ST | Serializability |
| | 2ND | SECURITY ANDINTEGRITY |
| | 3RD | Authorization and views |
| | 4TH | Authorization and views |
| 15TH | 1ST | Security constraints |
| | 2ND | Security constraints |
| | 3RD | Integrity Constraints |
| | 4TH | Discuss Encryption |

MSubudhi 13/2/2023
Signature of Faculty

MSubudhi 13/2/2023
HoD(I/c)
CSE Dept